REMARKS

Claims 1-22, 24, and 30-31 are in the application of which claims 1, 20, and 30 are in independent form. Claims 23 and 25-29 are cancelled.

The Examiner is thanked for the careful attention to detail he gave the application and in discovering several errors.

Request for an Interview. Attorney, Alan Aldous, requests a telephone interview. He can be reached at 503.264.7125.

Information Disclosure Statements. Supplemental Information Disclosure Statements were filed on December 12, 2002 and December 27, 2002. An additional supplemental Information Disclosure Statement is being filed concurrently herewith.

Claim objections: The claims are amended as suggested except that in claim 20, the word "data" is deleted from "data path." The paths certainly could carry data, but are not restricted to being only data paths.

35 U.S.C. § 112, 2nd paragraph rejections. Claims 1, 4-6, 10, 21, and 23 stand rejected under 35 U.S.C. § 112, 2nd paragraph, as being indefinite.

In claim 1, line 12, "first module" is changed to "second module." That is, each module has first and second chips. An example is found in FIG. 30, although the invention is not limited to these details. Note in FIG. 30, the on die terminations for chips I8 and I16 in module 1 are disabled and the on die terminations for chips I7 and I15 in module 2 are enabled.

Regarding claims 4 and 5, R-termination elements and an R-termination network are shown in FIGS. 32 and 33. An R-termination network is also shown in FIG. 34, although the inventions are not limited to the details of FIG. 32 or FIG. 33. "R-termination" means resistive termination. As a practical matter, the resistance probably would be constructed from transistors, but the resistance could be provided from something else. It is believed that the claims are definite.

Claims 6 and 10 are amended to delete reference to the second and fourth paths, respectively.

Claim 21 is amended to recite first and second paths.

Claim 23 is cancelled.

Double patenting. Claims 25-29 are cancelled. The Examiner is thanked for noticing this error.

35 U.S.C. § 102(b) rejections. Claims 30 and 31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Patent 5,467,455 to Gay et al.

Claim 30 is amended to recite:

"selectable on die termination coupled to the stub and load, wherein the on die termination includes multiple field effect transistors that can be individually turned on or off to create a desired termination impedance and the DRAM further comprises a linearized active resistive termination bias circuit coupled to control inputs for at least some of the field effect transistors."

This linearized active resistive termination bias circuit is not taught by Gay et al. For an example, see linearized active R-term network bias circuit 410 is shown in FIG. 32 and 33 of the present application. Accordingly, the rejection of claim 30 and 31 should be withdrawn.

Claims 20-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent 6,438,012 to Osaka et al.

Claim 20 recites that a first path is terminated in an on module termination in a second module and a second path is terminated in an on module termination in a first module. By contrast, the path (main line 1-1?) in FIG. 1 is terminated on the motherboard in the right hand side of the figure. If the terminations of lines 1-2, 1-3, etc., could be considered terminations of the path, Osaka et al. still would not show different paths being terminated in different modules.

Accordingly, the rejection of claim 20 and dependent claims 21-23 should be withdrawn.

35 U.S.C. § 103(a) rejections.

Claims 1, 2, 4-7, 10-13, 15-17, 19, 30, and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Patent 6,026,456 to Ilkbahar.

The Office action, p. 9, cites col. 7, lines 61-65, and col. 8, lines 49-57, to suggest it would be obvious for to disable terminations of chips in one module, while enabling chips in another module. However, these sections of Ilkbahar do not teach this. These sections refer to FIG. 5 of Ilkbahar. FIG. 5 is processor 112 including a suitable termination circuit as well as an output driver circuit, but the termination circuit is not restricted to use with processors. (Col. 7, lines 46-50.) Col. 7, lines 61-65, states:

"The termination circuit further comprises a process compensation circuit 510 and a control circuit 520. The processor 112 also includes the output driver which comprises a pullup 530

controlled by a control bus 526 and a pulldown 550 controlled by a control bus 522."

Col. 8, lines 49-57 states:

"In order to drive the low voltage, the control circuit enables the pulldown 550 and disables the pullups 530, 540, and 560. To drive the high voltage, the control circuit enables the pullup 530 and disables the pulldown 550. The control circuit 520 enables the pullup 560 and the pullup 540 to terminate the interface node 555 unless the pulldown is enabled. The control circuit 520 may be configured to disable the termination pullups 540 and 560 at other times as well. For example, the termination on one of the bus agents of a DOT system could be disabled if other terminations in the system provide sufficient noise attenuation.

Accordingly, the distributed on-chip termination scheme can disable terminations at least when the chip driver and the on-chip termination would otherwise be in contention. Intelligent control of the terminations thereby yields power savings relative to a system with constantly enabled terminations. The integration of the terminations onto the chip makes possible such intelligent termination control by providing practical access to appropriate control circuits."

It is respectfully asserted that these do not support the conclusion that "the die terminations of the first and second chips 324 of first module 322 are disabled and the on die terminations of first and second chips 334 of second module 332 are enabled." (Office action, p. 9, paragraph II.) It says nothing like that. Accordingly, the rejections of claim 1 and dependent claims 2, 4-7, 10-13, 15-17, 19 should be withdrawn.

As noted above, claim 30 is amended to recite:

"selectable on die termination coupled to the stub and load, wherein the on die termination includes multiple field effect transistors that can be individually turned on or off to create a desired termination impedance and the DRAM further comprises a linearized active resistive termination bias circuit coupled to control inputs for at least some of the field effect transistors."

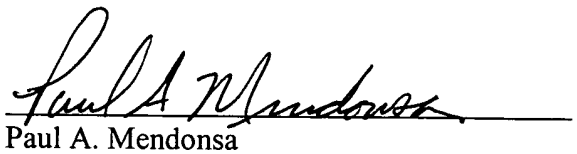
This linearized active resistive termination bias circuit is not taught by Ilkbahar. For an example, see linearized active R-term network bias circuit 410 is shown in FIG. 32 and 33 of the present application. Accordingly, the rejection of claim 30 and 31 should be withdrawn.

There are additional reasons why the claims are patentable.

Applicant believes the application is in condition for allowance and respectfully requests the same.

Respectfully submitted,

Dated: April 18, 2003



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